REMARKS

Claims 1-2, 4-17 and 20-22 are pending in this application. For purposes of expedition, claims 3 and 18-19 have been canceled without prejudice or disclaimer. Dependent claim 20 has been amended to incorporate all limitations of base claim 1 and base claim 18 (now canceled). Similarly dependent claims 5, 12, 13, 15, and 21-22 have been revised to depend upon the now independent claims 1 and 20. Entry of the foregoing amendments is proper under 37 C.F.R. §1.116(b) because claim 20 has simply been rewritten into independent form to include all limitations of base claim 18 which have already been considered by the Examiner, and claim 3, which has already been considered by the Examiner, has been incorporated into base claim 1. No new issues are raised; no further search is required; and the foregoing amendments are believed to remove the basis of the outstanding rejections and to place all claims in condition for allowance.

Turning now to the substance of the Office Action, claims 1-3 and 16-20 have been rejected under 35 U.S.C. §103(a) as being unpatentable over newly cited prior art, Ishii et al., U.S. Patent No. 5,973,749 in view of Melas, U.S. Publication No. 2002/0171961 for reasons stated on pages 2-3 of the Office Action. In support of the rejection of base claims 1 and 18, the Examiner cites FIG. 14, FIG. 17, elements 24c or 25k; col. 10, lines 52-65; col. 11, lines 5-12 and lines 38-40; of Ishii '749 for allegedly disclosing "a first signal processor nonlinearly converting the input signal based on a result of comparing an absolute value of the input signal and a predetermined critical value." The Examiner then admits that Ishii '749 does **not** disclose "a second signal processor [sic, detecting circuit] detecting binary data from the nonlinearly converted signal." However, the Examiner cites FIG. 2, element 210 and paragraph [0034] of Melas '961 for allegedly disclosing this feature.

However, the Examiner's assertion is factually incorrect. As previously discussed, claims 18-19 have been canceled and claim 20 has been amended to incorporate all limitations of base claim 18 (now canceled). Likewise, base claim 1 has been amended to incorporate all limitations of claim 3 (now canceled). As a result, the rejection of base claims 1 and 18 is now moot.

Moreover, even without new limitations which are now incorporated into base claims 1 and 20, Applicants submit that features of base claims 1 and 18, as previously presented, are

not disclosed or suggested by Ishii '749 and Melas '961, and request the Examiner to reconsider and withdraw this rejection for the following reasons.

In contrast to the Examiner's assertion, Ishii '749 discloses a letter-box screen detecting apparatus, as shown in FIG. 7, which can properly determine the presence/absence of a non-image portion and accurately perform determination of a letter-box screen, as shown in FIG. 1 and FIGs. 2A-2D. According to Ishii '749, a letter-box screen, as shown in FIG. 1, contains black non-image portions P1 and P2 without any video above and below a main screen S in display on a screen with an aspect ratio of 4:3, or other aspect ratios, such as, 16:9 or a movie size, including 1.85:1 or 2.35:1. When a letter-screen video signal is poor in quality, the letter-box screen is difficult to ascertain. As a result, Ishii '749 proposes a new letter-box screen detection apparatus for accurately determining a letter-box screen from a video signal.

However, Ishii '749 does **not** disclose any apparatus for accurately detecting binary data from an input signal (information) from an optical recording medium. More importantly, Ishii '749 does **not** disclose or suggest Applicants' claimed "a first signal processor nonlinearly converting the input signal based on a result of comparing an absolute value of the input signal and a predetermined critical value" as defined, for example, in base claim 1 (also see previously presented base claim 18).

The cited FIG. 14 of Ishii '749 shows the details of a vertical deflection circuit included in the letter-box screen detection apparatus. The cited FIG. 17 of Ishii '749 shows the details of a time-direction change detection circuit, including several nonlinear circuits 25k-25m. The cited column 10, lines 52-65 of Ishii '749 only describes the connection between the internal arrangement of the correlation detection circuit 24 and other blocks, as shown in FIG. 15. Likewise, column 11, lines 5-12 of Ishii '749 refers to the details of a time-direction change detection circuit 25, shown in FIG. 17.

Again, none of the cited portion of Ishii '749 discloses or suggests Applicants' claimed "a first signal processor nonlinearly converting the input signal based on a result of comparing an absolute value of the input signal and a predetermined critical value" as defined in base claim 1 (also see previously presented base claim 18), which advantageously improves the modulation and enhances data reproduction from an optical recording medium.

As a secondary reference, Melas '961 does **not** remedy the noted deficiencies of Ishii '749 in order to arrive at Applicants' base claim 1 (also see previously presented base claim 18). This is because Melas '961 only discloses a data detection circuit that is similar to that disclosed

in the Background of Applicants' disclosure. For example, FIG. 1 of Applicants' disclosure illustrates a data detection circuit that comprises an A/D converter 110, a Viterbi decoder 150 and an equalizer 140 disposed between the A/D converter 110 and the Viberti decoder 150 to compensate for an error included in digital data without DC offset. Similarly to FIG. 1 of Applicants' disclosure, the data detection circuit of Melas '961 also comprises an A/D converter 206, a Viberti decoder (including both PRML detector 210 and decoder 212), and a pair of linear and non-linear equalizers 208 and 214 disposed between the A/D converter 206 and the Viberti decoder 210, 212. According to Melas '961, the linear equalizer 208 is used to adjust the amplitude and phase relations of the sampled signal, and the nonlinear equalizer 214 is used to output a partial response sampled signal having two nonzero samples.

However, there is **no** disclosure from Melas '961 of Applicants' claimed "[first signal processor] nonlinearly converting the input signal based on a result of comparing an absolute value of the input signal and a predetermined critical value" as expressly defined in base claim 1 (also see previously presented base claim 18).

Moreover, there is **no** reason for one skilled in the art to modify the letter-box screen detecting apparatus of Ishii '749 to incorporate features from Melas '961 in the manner suggested by the Examiner, and even if so incorporated, the proposed incorporation still does not arrive at Applicants' base claim 1 (also see previously presented base claim 18).

In view of these reasons, Applicants respectfully request that the rejection of claims 1-3 and 16-20 be withdrawn, noting that claim 20, as amended, now further defines the specific of how an absolute value of the digital signal and a predetermined critical value are used to output a nonlinearly converted signal, features that are further not disclosed or suggested by Ishii '749 and Melas '961.

With respect to dependent claims 2 and 19, and dependent claims 3 and 20, the Examiner asserts that somehow Ishii '749 and Melas '961 disclose a specific type of nonlinear filter used, that is, the input [digital] signal is saturated when the absolute value of the input [digital] signal is larger than the predetermined critical value, and the input [digital] signal is output as the nonlinearly converted signal when the absolute value of the input [digital] signal is smaller than the predetermined critical value, and that the first signal processor outputs "a difference of the absolute value of the input signal and the critical value when the absolute value of the input signal is bigger than the critical value and outputs zero when the absolute value of the input signal is smaller than the critical value". The Examiner cites paragraphs [0031]-[0033]

of Melas '961 to support this assertion. However, the Examiner's assertion is misplaced and is incorrect for the following reasons.

Melas '961 only discloses the use of equalizers, and does **not** even disclose the use of non-linear converter to convert the input signal based on a result of comparing an absolute value of the input signal and a predetermined critical value, as defined in Applicants' base claims 1 and 18. As a result, there is **no** disclosure from Melas '961 of any nonlinear function based on two different types of nonlinear filters used, that is, when "a" is zero (0), as shown in FIGs. 6A-6B, or when "a" is one (1), as shown in FIGs. 6C-6D, as defined in Applicants' claims 2 and 19 and Applicants' claims 3 and 20.

There is simply **no** basis in fact for the Examiner to allege that Ishii '749 and Melas '961 disclose features of Applicants' claims 2 and 19 and Applicants' claims 3 and 20.

Similarly, with respect to claims 21 and 22, the Examiner also asserts that Melas '961 discloses the nonlinear function according to the equation as defined. However, for reasons discussed above, there is **no** disclosure from Ishii '749 and Melas '961 of any nonlinear function based on the specific equation as defined in Applicants' claims 21 and 22.

Lastly, claims 4-15 and 21-22 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Melas, U.S. Publication No. 2002/0171961 in view of Raz, U.S. Patent No. 6,639,537 for reasons stated on pages 5-7 of the final Office Action. Since this rejection is predicated upon the correctness of the rejection of Applicants' base claims, Applicants respectfully traverse these rejections primarily based on the same reasons discussed against the rejection of their base claim 1.

Moreover, claim 7 defines a specific arrangement of a first signal processor, as shown, for example, in FIG. 4, including: at least one finite impulse response (FIR) filter arranged to change frequency characteristics of the input signal; and a nonlinear filter arranged to generate the nonlinearly converted signal based on the absolute value of the input signal and the predetermined critical value. Even if Raz '537 discloses what the Examiner alleges, which Applicants do not believe, the incorporation of Raz '537 into Ishii '749 and Melas '691 does not arrive at Applicants' claim 7, and can only destroy the intended purposes of Ishii '749, which is to detect a letter-box screen of a video signal.

Separately, claim 8 alternatively defines a specific arrangement of a first signal processor, as shown in FIG. 9, including: first and second finite impulse response (FIR) filters

arranged in series to change frequency characteristics of the input signal; and a nonlinear filter disposed between the first and second FIR filters, to generate the nonlinearly converted signal based on the absolute value of the input signal and the predetermined critical value. Again, even if Raz '537 discloses what the Examiner alleges, which Applicants do not believe, the incorporation of Raz '537 into Ishii '749 and Melas '691 does not arrive at Applicants' claim 8, and can only destroy the intended purposes of Ishii '749, which is to detect a letter-box screen of a video signal.

Claim 11 alternatively defines a specific arrangement of a first signal processor, as shown in FIG. 10, including: a nonlinear filter to generate the nonlinearly converted signal based on the absolute value of the input signal and the predetermined critical value; and finite impulse response (FIR) filters arranged in front, behind and in parallel with the nonlinear filter respectively, to change frequency characteristics of the input signal. Again, even if Raz '537 discloses what the Examiner alleges, which Applicants do not believe, the incorporation of Raz '537 into Ishii '749 and Melas '691 does not arrive at Applicants' claim 11, and can only destroy the intended purposes of Ishii '749, which is to detect a letter-box screen of a video signal.

Claim 12 defines another specific arrangement of a first signal processor, as shown in FIG. 11, including: a nonlinear filter to generate the nonlinearly converted signal based on the absolute value of the input signal and the predetermined critical value; and finite impulse response (FIR) filters arranged behind and in parallel with the nonlinear filter respectively, to change frequency characteristics of the input signal. Again, even if Raz '537 discloses what the Examiner alleges, which Applicants do not believe, the incorporation of Raz '537 into Ishii '749 and Melas '691 does not arrive at Applicants' claim 12, and can only destroy the intended purposes of Ishii '749, which is to detect a letter-box screen of a video signal.

Claim 13 defines yet another specific arrangement of a first signal processor, as shown in FIG. 13, including: a nonlinear filter to generate the nonlinearly converted signal based on the absolute value of the input signal and the predetermined critical value; first and second finite impulse response (FIR) filters arranged in series behind with the nonlinear filter; and a third FIR filter arranged in parallel with the nonlinear filter, wherein the first, second and third FIR filters are configured to change frequency characteristics of the input signal. Again, even if Raz '537 discloses what the Examiner alleges, which Applicants do not believe, the incorporation of Raz '537 into Ishii '749 and Melas '691 does not arrive at Applicants' claim 13, and can only destroy the intended purposes of Ishii '749, which is to detect a letter-box screen of a video signal.

In view of the foregoing amendments, arguments and remarks, all claims are deemed to

be allowable and this application is believed to be in condition to be passed to issue. Should any questions remain unresolved, the Examiner is requested to telephone Applicants' attorney at the Washington DC office at (202) 216-9505. Applicants respectfully reserve all rights to file subsequent related application(s) (including reissue applications) directed to any or all previously claimed limitations/features which have been amended or canceled, or to any or all limitations/features not yet claimed, i.e., Applicants have no intention or desire to dedicate or surrender any limitations/features of the disclosed invention to the public.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage of fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of Stein, McEwen & Bui, LLP, No. 503333, and credit any excess fees to said deposit account.

Respectfully submitted,

STEIN, MCEWEN & BUI, LLP

Date: 4/23/08

By: _____
Hung H. Bui
Registration No. 40,415

1400 Eye St., NW
Suite 300
Washington, D.C. 20005
Telephone: (202) 216-9505
Facsimile: (202) 216-9510